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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,712	RHODES ET AL.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-28,54-59 and 61-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9,11-16,18-20,22-28,54-58,62,64,66,68 and 74-77* is/are rejected.

7)☒ Claim(s) *6, 8, 10, 17, 21, 59, 63, 65, 67, 69-73* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 4, 5, 9, 11-14, 16, 18-20 and 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Merrill et al. (US 2005/0087829 A1).

In re claim 1, Merrill (esp. Fig. 8) discloses a semiconductor device, comprising:

a semiconductor substrate (40) of a first conductivity type having a surface;

a gate (54) over a surface of the substrate; and

a photodiode within said substrate, said photodiode including an implant region of a second conductivity type, a first portion (46) of which extends further towards a region of said substrate beneath said gate than a second portion (51) of said implant region.

In re claim 2, Merrill discloses the device of claim 1, wherein the substrate is p-type and the implants are n-type.

In re claim 4, Merrill discloses the device of claim 1, wherein an upper portion of said implant region is farther away from the region beneath said gate than the other portions of the implant.

In re claim 5, Merrill discloses the device of claim 1, wherein the implant region includes a first portion (51), said first portion being nearest the substrate surface in the implant region.

In re claim 9, Merrill discloses the device of claim 1, wherein the implant region includes a third portion (41), said third portion being underneath the second portion in the implant region.

In re claims 11 and 13, Merrill discloses the device of claim 9. The limitation, "wherein ... are formed ... degrees" refers to the process for making this product and does not further distinguish the claimed structure over the prior art. In general, product-by-process claim language is not given patentable weight unless definite structural limitations are included to distinguish the claimed structure from that known to the prior art.

In re claim 12, Merrill discloses the device of claim 11, wherein the third portion (41) extends further than the first and second portions towards the region of said substrate beneath the gate.

In re claim 14, Merrill discloses the device of claim 12. The limitation, "wherein ... are formed ... degrees" refers to the process for making this product and does not further distinguish the claimed structure over the prior art. In general, product-by-process claim language is not given patentable weight unless definite structural

limitations are included to distinguish the claimed structure from that known to the prior art.

In re claim 16, Merrill discloses the device of claim 9, wherein the implant region includes a fourth portion (47), said fourth portion being lateral to the second portion in the direction of the gate.

In re claim 18, Merrill discloses the device of claim 16, wherein the fourth portion extends further than the first, second, and third portions towards the region of said substrate beneath said gate.

In re claims 19 and 20, Merrill discloses the device of claim 18. The limitation, "wherein ... are formed ... degrees" refers to the process for making this product and does not further distinguish the claimed structure over the prior art. In general, product-by-process claim language is not given patentable weight unless definite structural limitations are included to distinguish the claimed structure from that known to the prior art.

In re claim 22, Merrill discloses the device of claim 1, wherein the image pixel structure is a CCD imager (section [0110]).

In re claim 23, Merrill discloses the device of claim 1, wherein the image pixel structure is a CMOS imager (section [0146).

In re claim 24, Merrill (esp. Fig. 2A) discloses the device of claim 23, wherein said semiconductor device is a multiple transistor

3. Claims 1, 4, 5 and 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Shim (US 2002/0175355 A1).

In re claim 1, Shim (esp. Fig. 3D) discloses a CMOS image sensor comprising:

a semiconductor substrate (30) of a first conductivity type having a surface;

a gate (35) over a surface of the substrate; and

a photodiode (37, 32), said photodiode including an implant region (32) of a second conductivity type, a first portion of which extends further towards a region of said substrate beneath said gate than a second portion of said implant portion,

wherein said second portion is adjacent to and substantially underneath said first portion.

In re claim 4, Shim disclose the device of claim 1, wherein an upper portion (37) of said implant is farther away from the region beneath said gate than the other portions

In re claim 5, Shim disclose the device of claim 1, wherein the implant region includes a first portion (37), said first portion being nearest the substrate surface in the implant region.

In re claim 23, Shim disclose the device of claim 1, wherein the image pixel sensor is a CMOS imager.

In re claim 24, Shim disclose the device of claim 23, wherein the image pixel structure is one of a multiple transistor structure (as known to Shim at the time of the invention as shown in prior art Fig. 1).

4. Claims 1, 2, 4, 5, 9, 11, 15 and 22-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura et al. (US 2004/0108502 A1).

In re claim 1, Nakamura (esp. Fig. 9) discloses an image pixel structure, comprising:

a semiconductor substrate (32) of a first conductivity type having a surface;

a gate (42) over a surface of the substrate; and

a photodiode (36, 40, 50), said photodiode including an implant region (50) of a second conductivity type, a first portion of which extends further towards a region of said substrate beneath said gate than a second portion (40) of said implant portion,

wherein said second portion is adjacent to and substantially underneath said first portion.

In re claim 2, Nakamura discloses the device of claim 1, wherein the substrate is p-type and the implants are n-type.

In re claim 4, Nakamura discloses the device of claim 1, wherein an upper portion (36) of said implant is farther away from the region beneath said gate than the other portions

In re claim 5, Nakamura discloses the device of claim 1, wherein the implant region includes a first portion (36), said first portion being nearest the substrate surface in the implant region.

In re claim 9, Nakamura discloses the device of claim 1, wherein the implant region includes a third portion (40), said third portion being underneath the second portion in the implant region.

In re claims 11 and 13, Nakamura discloses the device of claim 9. The limitation, "wherein ... are formed ... degrees" refers to the process for making this product and does not further distinguish the claimed structure over the prior art. In general, product-by-process claim language is not given patentable weight unless definite structural limitations are included to distinguish the claimed structure from that known to the prior art.

In re claim 15, Nakamura discloses the device of claim 11, wherein the second portion (50) extends further than the first (36) and third (40) portions towards the region of said substrate beneath said gate.

In re claim 21, Nakamura discloses the device of claim 1. The limitation, "wherein ... are angled" is a product-by-process claim which does not further limit the structure of the claimed invention.

In re claim 22, Nakamura discloses the device of claim 1, wherein the image pixel sensor is a CCD imager (section [0227]).

In re claim 23, Nakamura disclose the device of claim 1, wherein the image pixel sensor is a CMOS imager (section [0227]).

In re claim 24, Nakamura (esp. Fig. 28) discloses the device of claim 23, wherein the image pixel structure is one of a multiple transistor structure.

In re claim 25, Nakamura discloses the device of claim 1, wherein the gate includes a gate oxide and a conductor.

In re claim 26, Nakamura discloses the device of claim 25, wherein the gate contains polysilicon (section [0245]).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (as above).

In re claim 3, Nakamura discloses the device of claim 1, wherein the substrate is p-type and the implants are n-type, but does not expressly disclose the substrate being n-type and the implants being p-type. To provide the device of Nakamura with a proportional reversal of conductivity types, respectively, would have been obvious to one of ordinary skill in this art because the reversal of material conductivity and potential is obvious to one of ordinary skill in this art since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. *In re Leshin*, 125 USPQ 416.

In re claims 27 and 28, Nakamura discloses the device of claim 1, but does not expressly disclose an insulator layer over the gate. Oxide interlayer insulating layers (ILLs) are well known in the art and it would have been obvious for one of ordinary skill in the art at the time of the invention to use such a layer over the gate conductor for the purpose, for example, of shielding and insulating the conductor from external connections.

7. Claims 9, 11, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shim as applied to claim 1 above, and further in view of Lee et al. (US 2003/0030083 A1).

In re claim 9, Shim disclose the device of claim 1, but does not expressly disclose a third portion underneath the second portion. Lee (esp. Fig. 2) discloses a third portion (201), said third portion being underneath the second portion (202) in the implant region. It would have been obvious for one skilled in the art to use a deep third region as disclosed by Lee for the device of Shim for the purpose, for example, of creating a deeper depletion region for the purpose, for example, of increasing the charge storage capacity of the pixel region.

In re claims 11 and 13 Shim in view of Lee discloses the device of claim 9. The limitation, "wherein ... are formed ... degrees" refers to the process for making this product and does not further distinguish the claimed structure over the prior art. In general, product-by-process claim language is not given patentable weight unless definite structural limitations are included to distinguish the claimed structure from that known to the prior art.

In re claim 15, Shim in view of Lee discloses the device of claim 11, wherein the second portion extends further than the first and third portions towards the region of said substrate beneath said gate.

8. Claims 54-58, 60, 62, 64, 66, 68 and 74-77 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura et al. (US 2004/0108502 A1) in view of Nagata et al. (U.S. Patent No. 6,407,417).

In re claim 54 Nakamura (esp. Fig. 9) discloses a CMOS image pixel structure, comprising:

a semiconductor substrate (32) of a first conductivity type having a surface;

a gate (42) over a surface of the substrate; and

a photodiode (36, 40, 50), said photodiode including an implant region (50) of a second conductivity type, a first portion of which extends further towards a region of said substrate beneath said gate than a second portion (40) of said implant portion,

wherein said second portion is adjacent to and substantially underneath said first portion.

Nakamura does not expressly disclose the CMOS imaging device also comprising a processor. Nagata (esp. Fig. 13) discloses a photoelectric conversion device similar to that of Nakamura that makes use of a processor. It would have been obvious to one skilled in the art at the time of the invention to use a processor as disclosed by Nagata for the device of Nakamura for the purpose, for example, of better controlling the various modes.

In re claim 55, Nakamura in view of Nagata discloses the device of claim 54, wherein the substrate is p-type and the implants are n-type.

In re claim 56, Nakamura in view of Nagata discloses the device of claim 54, wherein the substrate is p-type and the implants are n-type, but does not expressly

disclose the substrate being n-type and the implants being p-type. To provide the device of Nakamura with a proportional reversal of conductivity types, respectively, would have been obvious to one of ordinary skill in this art because the reversal of material conductivity and potential is obvious to one of ordinary skill in this art since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. *In re Leshin*, 125 USPQ 416.

In re claim 57, Nakamura in view of Nagata discloses the device of claim 54, wherein an upper portion (36) of said implant is farther away from the region beneath said gate than the other portions

In re claim 58, Nakamura in view of Nagata discloses the device of claim 54, wherein the implant region includes a first portion (36), said first portion being nearest the substrate surface in the implant region.

In re claim 60, Nakamura in view of Nagata discloses the device of claim 58, wherein the implant region includes a second portion (50), said second portion being underneath the first portion in the implant region.

In re claim 62, Nakamura in view of Nagata discloses the device of claim 60, wherein the implant region includes a third portion (40), said third portion being underneath the second portion in the implant region.

In re claims 64 and 66, Nakamura discloses the device of claim 62. The limitation, "wherein ... are formed ... degrees" refers to the process for making this product and does not further distinguish the claimed structure over the prior art. In general, product-by-process claim language is not given patentable weight unless

definite structural limitations are included to distinguish the claimed structure from that known to the prior art.

In re claim 68, Nakamura in view of Nagata discloses the device of claim 64, wherein the second portion (50) extends further than the first (36) and third (40) portions towards the region of said substrate beneath said gate.

In re claim 74, Nakamura in view of Nagata discloses the device of claim 54. The limitation, "wherein ... are angled" is a product-by-process claim which does not further limit the structure of the claimed invention.

In re claim 75, Nakamura in view of Nagata discloses the device of claim 54, wherein the image pixel sensor is a CCD imager (section [0227]).

In re claim 76, Nakamura in view of Nagata discloses the device of claim 54, wherein the image pixel sensor is a CMOS imager (section [0227]).

In re claim 77, Nakamura (esp. Fig. 28) in view of Nagata discloses the device of claim 76, wherein the image pixel structure is one of a multiple transistor structure.

Response to Arguments

1. Applicant's arguments filed 09/15/05 have been fully considered but they are not persuasive.

a. Applicant traverses the rejection under Merrill et al. (US 2005/0087829) on the grounds that Merrill does not disclose a "second portion adjacent to a first portion of the second conductivity type."

i. Examiner respectfully disagrees. The words, "adjacent to" do not mean "adjoining." Using the words, "adjacent to," applicant leaves open the possibility that two regions may be spaced apart from each other, so long as there is not a portion of the same region in the space there between[1].

ii. Section [0066] of Merrill describes how photodiodes are created in the alternating P/N junctions of the regions shown in Fig. 8. Because the implant regions 41, 46 and 51 are not separated by any other implant regions, they can be interpreted as being "adjacent to" one another. Moreover, if one looks at the region just below the gate region (54), the regions 41, 46 and 51 are clearly adjacent to one another.

iii. Secondly, the implant region (46) for example, can be seen as encompassing two different regions, which also meet the claim. The first region of the region (46) would be the vertical portion, and the second portion would be the underlying horizontal portion. Such layers are adjacent one another and one of the regions (the vertical first) extends farther under the gate than the second (horizontal second.)

b. Second, Applicant traverses the rejection under Shim (US 20020175355) on the grounds that Shim does not disclose a "first and second portion of an implant region of a second conductivity type."

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[1] Adjacent is defined as "not distant" and "nearby." Syn Adjacent, Adjoining, Contiguous, Juxtaposed mean being in close proximity. Adjacent may or may not imply contact but always implies absence of anything of the same kind in between. Adjoining definitely implies meeting and touching at some point or

iv. In this case, applicant's choice of modifying clauses leaves room for interpretation. The key phrases being, "said photodiode including an implant region of a second conductivity type, a first portion of which..."

(1) Notably, the claim language does not require that the photodiode be entirely of one conductivity type. The term, "including" is interpreted to mean that the photodiode "comprises" a region of a second conductivity type, but it may also comprise/include regions of other conductivity types. Therefore, the photodiode region of Shin includes both regions (37 and 32). The "second region" portion" (32) of Shim being clearly below the first portion (37).

(2) Secondly, the phrase, "a first portion of which" does not clearly indicate which subject it is modifying. Where there is ambiguity in the claim language, the examiner must read the claim in its broadest possible sense. In this case, where interpreted by the examiner, "a first portion of which" is modifying the photodiode, not the implant region. Therefore, the photodiode may comprise several different implant regions of varying conductivity types, while the implant region is a separate implant region of one conductivity type.

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line. Contiguous implies having contact on all or most of one side. Juxtaposed means placed side by side esp. so as to permit comparison and contrast. Merriam-Webster's Collegiate Dictionary, 1997

c. Lastly, the similar broad interpretation is applied to the interpretation of the claim in light of the Nakamura et al. (US 2004/0108502) reference. Again, the claim language does not require that the photodiode be entirely of one conductivity type. The term, "including" is interpreted to mean that the photodiode "comprises" a region of a second conductivity type, but it may also comprise/include regions of other conductivity types. The photodiode region of Nakamura includes all three regions (36, 40 and 50). The "second region" portion" (40) of Nakamura is clearly "substantially underneath" the first portion (50) as shown in several embodiments, notably, Fig. 11C.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815

JEROME JACKSON
PRIMARY EXAMINER